WHAT IS CLAIMED IS:

1. A wireless Crest Factor reduction circuit for use with multi-carrier signals in a wireless communication system to enhance the linearity and performance of the amplifier, in particular wireless cellular, PCS, wireless LAN, line of sight microwave, military, and satellite communication systems and any other none wireless applications, the Crest Factor reduction circuit comprising:

-   A multi-carrier receiver for the Crest Factor reduction of IF or RF input signal to amplifier. If the input signal is baseband then the multi-carrier receiver is bypassed.

-   A digital signal processing block to reduce the Crest Factor of the multi-carrier input signal.

-   A digital signal processing block to limit or clip the amplitude of the multi-carrier signal.

-   A digital signal processing block that converts the amplitude clipped or limited multi-carrier baseband to baseband representative of individual carrier signals..

-   A digital signal processing block that filters the baseband representative of individual carrier baseband signal to remove unwanted signal produced due to clipping or limiting the multi-carrier signal amplitude.

-   A digital signal processing signal that up converts the filtered baseband representative of each carrier to its original baseband frequency.

-   A multi-carrier transmitter block that prepare the Crest Factor reduced multi-carrier signal for delivery to multi-carrier amplifier.

2. The Crest Factor reduction circuit according to claim 1, wherein multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency.

3. The Crest Factor reduction circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency and the digitized multi-carrier input signal is decimated to the appropriate number of samples per symbol for further digital signal processing.

4. The Crest Factor reduction circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is baseband and is sampled using Nyquist sampling technique and interpolated to produce the baseband multi-carrier signal with appropriate number of samples per symbol.

5. The Crest Factor reduction circuit according to claim 1, wherein the multi-carrier input signals from the wireless transmitter are in bit domain and the bit domain baseband signals are up converted, combined and interpolated to produce the digital multi-carrier baseband signal with appropriate number of sample per symbol.

6. The Crest Factor reduction according to claim 1, wherein the digital multi-carrier signal is amplitude clipped or limited by a limiting or clipping function. The amplitude limited multi-carrier signal is then down converted to single channel baseband signals by digital down conversion. The individual baseband signals are filtered and up converted back to their original baseband frequency before all individual baseband signals being combined again to produce the multi-carrier Crest Factor reduced baseband signal.

7. The Crest Factor reduction according to claim 1, wherein the multi-carrier signal amplitude clipping or limiting can be perform in analog domain at an

intermediate frequency (IF) , radio frequency, or analog baseband before being digitized.

8. The Crest Factor reduction according to claim 1, wherein the amplitude limited digital multi-carrier baseband signal is converted to single channel baseband signals by digital down conversion.

9. The Crest Factor reduction circuit according to claim 1, wherein the Crest Factor reduced signal is digitally up converted and converted to analog domain at an intermediate frequency or the output frequency.

10. The Crest Factor reduction circuit according to claim 1, wherein the received signal strength of the input signal to Crest Factor reduction circuit and transmit signal strength of the output from the Crest Factor reduction circuit is dynamically measures to adjust the total gain of the Crest Factor reduction circuit to zero

11. The Crest Factor reduction circuit according to claim 1 and subsequent claims, when it is used in wireless cellular, wireless PCS, wireless LAN, microwave, wireless satellite, none wireless amplifiers, and any wireless communication systems used for military applications.

12. The Crest Factor reduction circuit according to claim 1, wherein the DSP function can be implemented in programmable logic, FPGA, Gate Array, ASIC, and DSP processor